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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TREAT, WILLIAM M

ART UNIT PAPER NUMBER

2183

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/992,159

Applicant(s)

WONG ET AL.

Examiner

William M. Treat

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/6/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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1. Claims 1-22 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Tremblay et al. (Patent No. 6,279,100).
4. Tremblay taught the invention of exemplary claim 1 including a processor (cols. 25-26, claim 1) comprising a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing an instruction on successive clock cycles (col. 26, claim 6); and stall control circuitry which controls the stalling of instructions in the pipelines in response to a stall signal generated in anyone of the pipelines (col. 26, claims 3 and 4); wherein the stall control circuitry is adapted to stall the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later than the execution of an instruction in a pipeline generating the stall signal, and to release the stall in the pipeline not generating the stall signal at least one clock cycle later than the stall in the pipeline generating the stall signal (col. 21, lines 18-26).
5. As to claim 2, the examiner interprets the language of claim 2 to say that if a pipeline has already stalled itself, the pipeline does not then allow another pipeline to also stall it in an interlocking fashion. Tremblay inherently taught this. If pipeline 1 stalled itself and on the next cycle sent a stall signal to pipeline 2 while pipeline 2 had simultaneously stalled itself and sent a stall signal on the next cycle to pipeline, they could become interlocked with each pipeline

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waiting on the other to send a stall-clear signal. Tremblay's system must inherently prevent such interdependence or it would not work.

6. As to claim 3, Tremblay inherently taught when pipeline stage I is stalled, stalling all previous stages in that same pipeline. Otherwise, data generated in, for instance, the decode stage would ultimately overlay data stalled in the execute stage and/or be lost rendering his invention useless.

7. As to claim 4, any decode stall which propagated from one media functional unit (220) to a second media functional unit (220) on a subsequent clock cycle would inherently find that the instruction in that pipeline had progressed to a subsequent pipeline processing stage.

8. As to claim 5, Tremblay taught the processor comprises a plurality of pipeline clusters and each cluster comprising a plurality of pipelines (col. 5, lines 35-65).

9. As to claims 6 and 7, Tremblay taught stalling execution of instructions in one cluster in one clock cycle and stalling execution of instruction in a second cluster's pipelines on subsequent clock cycles (Abstract, lines 1-4).

10. As to claim 8, Tremblay taught instructions entering the different pipelines in parallel exit in parallel (col. 5, lines 54-58).

11. As to claim 9, Tremblay taught different instructions are executed in different pipelines (col. 6, lines 39-43).

12. As to claim 10, Tremblay taught instructions from a VLIW instruction packet are issued in parallel to the pipelines (col. 6, lines 39-43).

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13. As to claim 11, Tremblay taught a processor in which each pipeline includes at least one execute stage in which an instruction is at least partially executed (col. 10, lines 41-47). With multiple execute stages in his pipelines there was partial execution in each stage.

14. As to claim 12, Tremblay did not flush the pipelines in response to the stall signal (see the entire patent).

15. As to claims 13 and 14, Tremblay taught the pipeline control circuitry distributed between two or more pipeline stages and stall control circuitry associated with two or more pipeline stages for controlling stalling of those stages (col. 24, lines 25-27 and lines 55-60). If one is able to stall the decode and execution stages with specific E-stage and D-stage stalls then there is pipeline stall control circuitry associated with each pipeline stage or one could not stall the stages.

16. As to claim 15, Tremblay taught generating a global stall signal for stalling another pipeline and inherently circuitry within the other pipeline to stall one or more of its stages (col. 26, claim 4).

17. As to claim 16, Tremblay taught the first stall signal generates the stall (Fig. 14).

18. As to claim 17, Tremblay taught his stall control circuitry being substantially the same (col. 6, lines 14-23).

19. As to claim 18, Tremblay taught the pipeline stage is not stalled if there is a bubble in that pipeline stage (col. 21, lines 26-34).

20. As to claims 19-22, they fail to teach or define over rejected claims

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claims 1 and 19-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Murty et al. (Patent No. 6,044,456).

23. The examiner would suggest applicants read cols. 8-9, claims 1-5 and 11 before responding.

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

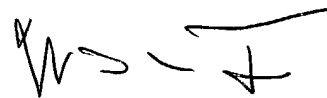
25. Gearty et al. (Patent No. 6,477,638).

26. Biswas et al. (Patent No. 5,860,000).

27. Soltis, Jr. et al. (Patent No. 6,587,940).

28. Any inquiry concerning this communication should be directed to William M. Treat at telephone number 703 305 9699. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER